Amendment to the Specification

Kindly amend the Specification as follows:

[0002] Spacers are common structures in complementary metal-oxide semiconductor (CMOS) processing provided to protect one structure from processing done to an adjacent structure. Exemplary types of CMOS devices in which protective spacers must be used are Fin Field Effect Transistors (FinFETs) and MesaFETs. A FinFET, for example, structurally includes, among other things, a gate that extends over and along a portion of each sidewall of a thin, vertical, silicon "fin." In FinFETS, a spacer is required for blocking implants at the gate edge and preventing silicide shorts to the gate. Conventional planar CMOS spacer processing presents a number of problems relative to the fin. In particular, conventional processing to form the spacer for the gate results in application to the fin. If conventional spacer processes are used, fin erosion during spacer etch is a potential problem. When the fin needs to be exceptionally thin, any additional etching can prevent attainment of the desired fin size. Another challenge is formation of a spacer along the gate without formation on the fin sidewalls and the top of the fin such that the part ~~the part~~ of the fin not adjacent to the gate can be exposed to implantation. In conventional spacer processing, a spacer formed on the gate also forms on the sidewalls of the fin due to the three-dimensional nature of the FinFET. In some cases, such as during sidewall implantation or source drain extension, this sidewall spacer is undesirable. Attempts to remove the fin sidewall spacer result in removing the spacer on the gate where a spacer is needed. Similar problems exist relative to other CMOS devices such as MesaFETs.

[0020] FIGS. 4A-B show a first embodiment in which second material 22 is formed (in the step shown in FIGS. 2A-B) as a polycrystalline silicon (hereinafter

'polysilicon') such that it has an oxidation rate faster than first material 20. In order to provide these differential oxidation rates, in one embodiment, second material 22 may be a portion of first material 20 that is implanted with a dopant in a known fashion. The dopant may be any material that causes polysilicon second material 22 to oxidize at a faster rate than non-doped polysilicon. The dopant may be, for example, Arsenic (As) (preferred), Germanium (Ge), Cesium (Cs), Argon (Ar) or ~~Flourine~~ Fluorine (F) or a combination thereof. In another embodiment, second material 22 that has a faster oxidation rate than first material 20 may be deposited on the first material, e.g., as polycrystalline silicon-germanium alloy. First material 20 may be, for example, non-doped polysilicon. According to this embodiment, second material 22 is made to overhang first material 20 by conducting an oxidation, e.g., at 800 to 950°C. The differential oxidation rate between materials generates a thicker oxide from second material 22 of gate structure 24 relative to fin 14 and first material 20. The result is generation of an overhang 40 of fin 14 adjacent to first material 20. FIGS. 4A-B show the resulting structure in which second material 22 forms a top portion 30 of gate structure 24 that overhangs an electrically conductive lower portion 32 thereof. The oxidation process may also cause thin oxide layers 34 (e.g., approximately ten times thinner than second material 22) to form on the sides of first material 20 (i.e., lower portion 32) and the sides of fin 14 outside of gate structure 24. Oxide layer 34 allows for preservation of fin 14 width without oxidizing the fin away.

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